Notice of Allowability	Application No.	Applicant(s)	
	09/873,820	SONG, HONGJIANG	
	Examiner	Art Unit	
	Khanh Tran	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *06/04/2001*.

2. ☒ The allowed claim(s) is/are *1-20*.

3. ☒ The drawings filed on *04 June 2001* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

TESFALDET BOCURE
PRIMARY EXAMINER

Reasons for Allowance

The following is an examiner's statement of reasons for allowance:

The present invention is directed to a signal delay circuit that compensates for other delays introduced within the signal delay circuit itself. The signal delay circuit comprises *a synchronization circuit* for determining a first selection value that selects a first delayed clock, whose delay compensates for the propagation delays created in a selection circuit, and a *selection circuit* for adding a specified offset value to the first selection value and using the result to select a second delayed clock whose delay approximates the sum of the internal delay of the selection circuit and the delay specified by the offset value. Each independent claim identifies the critical features, which distinct the invention from the cited prior art of record. The cited prior art of record does not compensate for additional delays (e.g. the specified offset value) that occur *after the synchronized clock signals are produced.*

1. Regarding claim 1, claim 1 is allowed over the prior art of record since the cited references taken individually or in combination fails to particularly disclose an apparatus comprising "*a selection circuit to receive an offset value ..., the selection circuit ... having an output load to output data timed with a first selected one of the multiple delayed output clock signals*" and "*a synchronization circuit having a load simulation circuit to simulate the output load ...*". It is noted that the closest prior art, Gersbach et al. (US 5,245,637) disclosing a digital phase lock logic system which

compensates for changes in both phase and frequency of a received composite clock and data signal, either singularly or in combination, fail to anticipate or render the above underlined limitations obvious.

2. Regarding claim 8, claim 8 is allowed over the prior art of record since the cited references taken individually or in combination fails to particularly disclose a system comprising a clock delay control circuit including "*a selection circuit to receive an offset value ..., the selection circuit ... having an output load to output data timed with a first selected one of the multiple delayed output clock signals*" and "*a synchronization circuit having a load simulation circuit to simulate the output load ...*". It is noted that the closest prior art, Gersbach et al. (US 5,245,637) disclosing a digital phase lock logic system which compensates for changes in both phase and frequency of a received composite clock and data signal, either singularly or in combination, fail to anticipate or render the above underlined limitations obvious.

3. Regarding claim 15, claim 15 is allowed over the prior art of record since the cited references taken individually or in combination fails to particularly disclose a method comprising the steps of "*producing an intermediate clock from an output simulation circuit that simulates at least one characteristic of an output signal*" and "*determining a selection value ... to synchronize the intermediate clock with a reference clock*" and "*adding an offset value to the selection value to select another of the delayed clock signals to provide an output signal from the output circuit*". It is noted that the

closest prior art, Gersbach et al. (US 5,245,637) disclosing a digital phase lock logic system which compensates for changes in both phase and frequency of a received composite clock and data signal, either singularly or in combination, fail to anticipate or render the above underlined limitations obvious.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Gersbach et al. U.S. Patent 5,245,637 discloses "Phase And Frequency Adjustable Digital Phase Lock Logic System".

Culley et al. U.S. Patent 6,182,236 B1 discloses "Circuit And Method Employing Feedback For Driving A Clocking Signal To Compensate For Load-Induced Skew".

Ozkan U.S. Patent 5,488,641 discloses "Digital Phase-Locked Loop Circuit".

Avaneas U.S. Patent 4,841,551 discloses "High Speed Data-Clock Synchronization Processor".

Schwartz et al. U.S. Patent 5,854,797 discloses "Tester With Fast Refire Recovery Time".

Ferraiolo et al. U.S. Patent 5,220,581 discloses "Digital Data Link Performance Monitor".

Buchanan et al. U.S. Patent 6,650,661 B1 discloses "System That Compensates For Variances Due To Process And Temperature Changes".

Wakayama et al. U.S. Patent 6,064,244 discloses "Phase-Locked Loop Circuit Permitting Reduction Of Circuit Size".

Kawasaki et al. U.S. Patent 6,066,969 discloses "Semiconductor Device With DLL Circuit Avoiding Excessive Power Consumption".

Guang-Kaai Dehng, June-Ming Hsu, Ching-Yuan Yang, Shen-luan Liu, "Clock-Deskew Buffer Using a SAR-Controlled Delay-Locked Loop", August 2000, IEEE Journal Of Solid-State Circuits, Volume 8, No. 8.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KCT